FEATURES

- **High performance, low power 8bit RISC core**
  131 Instructions, 80% execute in one cycle
  32x8 general purpose registers
  Up to 32MIPS when running at 32MHz
  Integrated one-cycle 8x8 Multiplier
- **Data and Programming Memory**
  8Kbytes In-system-programmable FLASH memory
  1Kbytes Internal SRAM
  504Bytes Data FLASH, Support Byte-wise access (E2PROM like)
  Creative flash encryption based on state changing.
- **Peripherals**
  Two 8bit Timer/Counter, support compare-match output
  One 16bit Timer/Counter with separated clock prescalar, Support Input Capture and compare-match output
  Internal 32 KHz RC oscillator, support calibrated to ±1%
  Up to 6-channel PWM
  8-channel 10bit Analog/Digital Converter
    - 3-channel Difference input, x7.5, x15, x30 gain control
    - Integrated thermal sensor
  2-channel Analog Comparator, channel can be extended from ADC
  Programmable Watch dog timer
  Programmable serial USART
  Master/slave SPI serial Interface
  Byte-oriented 2-wire serial interface (Philips I2C compatible)
- **Special Microcontroller features**
  Serial Wire on-chip Debug (SWD)
  External and internal interrupt sources
  Power on reset and 3-level Brown-out Reset (Low voltage reset)
  Internal 32 MHz RC oscillator, ±1% after calibration
  Internal 32 KHz RC oscillator, ±1% after calibration
  External crystal support 32.768 KHz or 400K~32MHz
  Up to 12-channel capacitive touch keys
  8-channel NMOS I/O, sink up to 80mA current.
- **I/O and Package**
  QFP32L (provide up to 30 GPIO)
  S/SOP28L (provide up to 26 GPIO)
- **Operating Environment**

Power supply:	1.8V ~ 5.5V
Frequency:	0 ~ 32MHz
Temperature:	-40C ~ +85C
HBM ESD:	4000V

LogicGreen

8-bit LGT8XM

RISC Microcontroller with 8192 Bytes In-System Programmable FLASH Memory

LGT8F88A

Data book

Version 1.1.1

Application

Kitchen

- Microwave oven
- Induction cooker
- Electric cooker

Smart home appliance

- Milk machine
- Coffee maker
- Water heater

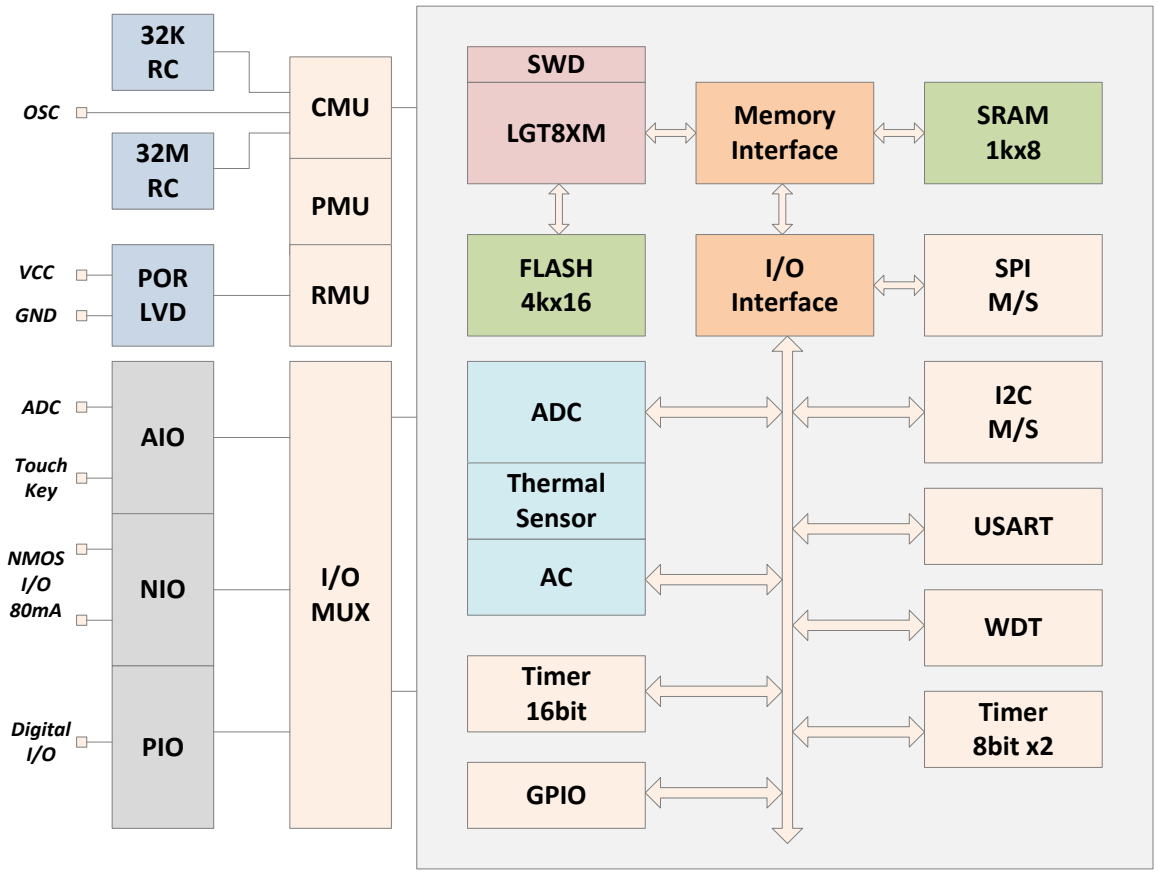
Smart control devices

- Li-on charger
- Motor control
- Smart toys

Hand-held device

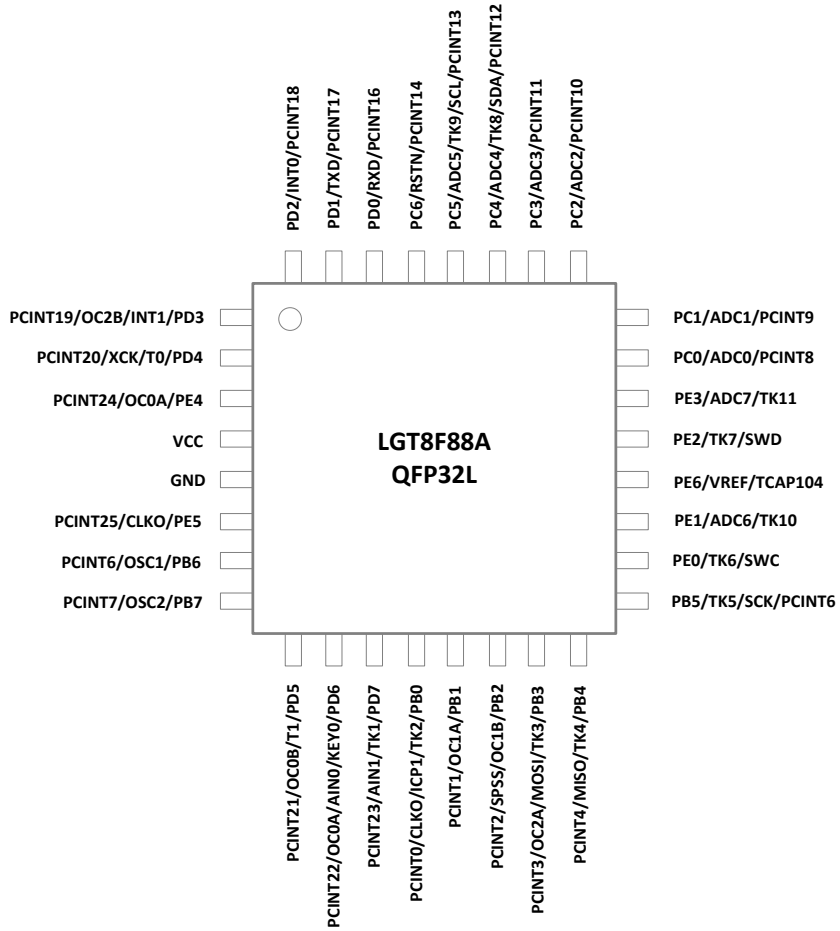
System Architecture

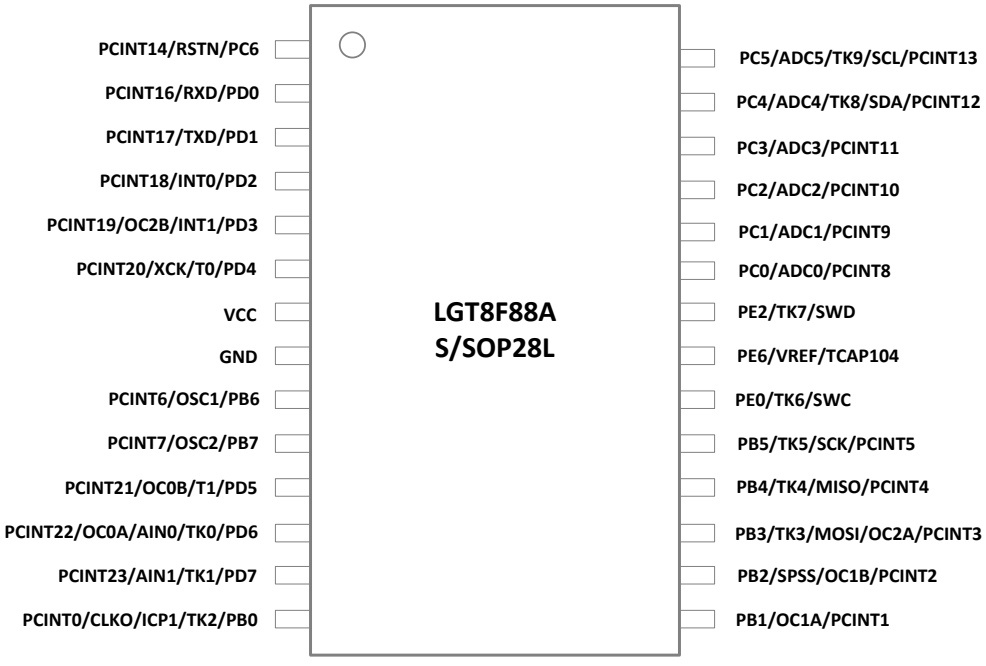
LGT8F88A Diagram



Module Name	Function Description
SWD	On-chip debugger
LGT8XM	8bit High performance RISC core
CMU	Clock management Unit
PMU	Power Management Unit
RMU	Reset Management Unit
POR/LVD	Power on Reset and Low voltage detector
ADC Thermal Sensor AC	8-channel 10bit ADC Thermal Sensor Analog Comparator
AIO NIO PIO	ADC and Touch Key inputs 80mA high sink NMOS I/O Programmable Digital I/O
WDT	Watch Dog Timer

Pin-out Assignment





Pin-out Definition

PIN Name	Function Description
VCC	Power supply (1.8V ~ 5.5V)
GND	System Ground
OSC1 **OSC2**	External Crystal or clock input
RSTN	External Reset input, low active
RXD **TXD** **XCK**	USART interface
INT0/1	External Interrupts or external wake-up sources
OC0A/B	Timer/Counter 0 compare-match output (PWM0A/B)
OC1A/B	Timer/Counter 1 compare-match output (PWM1A/B)
OC2A/B	Timer/Counter 2 compare-match output (PWM2A/B)
SCL **SDA**	Byte-oriented Two wire interface (I2C compatible)
SCK **SPSS** **MISO** **MOSI**	Master/Slave SPI interface
T0	External clock input of Timer0
T1	External clock input of Timer1
ICP1	Capture input of Timer1
SWD **SWC**	SWD on-chip debugger or ISP interface
PCINTX	Pin status change interrupts
ADC7…0	Analog input channels of ADC
TK11…0	Capacitive touch key inputs
VREF/TCAP104	External VREF of ADC External filter-capacitance (0.1uF) of Touch Key circuit
AIN0 **AIN1**	Input channel of Analog Comparator
CLKO	System clock output
PB7…0	Programmable General Purpose I/O
PD7…0	Programmable General Purpose I/O
PC6…0	Programmable General Purpose I/O
PE6…0	Programmable General Purpose I/O
PD5…0 **PE5…4**	NMOS I/O, Can be sink up to 80mA

REGISTERS INDEX

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Extended IO Register									
$F6	GUID3	GUID Byte 3							
$F5	GUID2	GUID Byte 2							
$F4	GUID1	GUID Byte 1							
$F3	GUID0	GUID Byte 0							
$F2	PMCR	PMCE	LFEN	EXTEN	WCES	OSCKEN	OSCMEN	RCKEN	RCMEN
$F1	DSCR	DSCE	-	-	DSC4	DSC3	DSC2	DSC1	DSC0
$F0	IOCR	IOCE	-	-	-	-	-	REFIOEN	RSTIOEN
$E2	PSSR	PSS1	-	-	-	-	-	-	PSR1
$CF	DIDR3	-	-	-	-	TIN11D	TIN10D	TIN9D	TIN8D
$CE	DIDR2	TIN7D	TIN6D	TIN5D	TIN4D	TIN3D	TIN2D	TIN1D	TIN0D
$CD	TKCSR	TKPD	TKPSEL			TKMUX			
$C6	UDR0	USART Data							
$C5	UBRR0H	-	-	-	-	USART Baud Rate Register High			
$C4	UBRR0L	USART Baud Rate Register Low							
$C2	UCSR0C	UMSEL0		UPM0		USBS0	UCSZ01/ UDORD0	UCSZ00/ UCPHA0	UCPOL0
$C1	UCSR0B	RXCIE0	TXCIE0	UDRIE0	RXEN0	TXEN0	UCSZ02	RXB80	TXB80
$C0	UCSR0A	RXC0	TXC0	UDRE0	FE0	DOR0	UPE0	U2X0	MPCM0
$BD	TWAMR	TWI Address Mask							-
$BC	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE
$BB	TWDR	TWI Data							
$BA	TWAR	TWI Address							TWGCE
$B9	TWSR	TWI Status					-	TWPS	
$B8	TWBR	TWI Bit Rate							
$B6	ASSR	-	EXCLK	AS2	TCN2UB	OCR2AUB	OCR2BUB	TCR2AUB	TCR2BUB
$B4	OCR2B	Timer/Counter 2 Output Compare Register B							
$B3	OCR2A	Timer/Counter 2 Output Compare Register A							
$B2	TCNT2	Timer/Counter 2 Counter Register							
$B1	TCCR2B	FOC2A	FOC2B	-	-	WGM22	CS2		
$B0	TCCR2A	COM2A		COM2B		-	-	WGM21	WGM20

$A9	PORTE	Port Output E							
$A8	DDRE	Data Direction E							
$A7	PINE	Port Input E							
$8B	OCR1BH	Timer/Counter 1 Output Compare B High							
$8A	OCR1BL	Timer/Counter 1 Output Compare B Low							
$89	OCR1AH	Timer/Counter 1 Output Compare A High							
$88	OCR1AL	Timer/Counter 1 Output Compare A Low							
$87	ICR1H	Timer/Counter 1 Input Capture High							
$86	ICR1L	Timer/Counter 1 Input Capture Low							
$85	TCNT1H	Timer/Counter 1 Counter High							
$84	TCNT1L	Timer/Counter 1 Counter Low							
$82	TCCR1C	FOC1A	FOC1B	-	-	-	-	-	-
$81	TCCR1B	ICNC1	ICES1	-	WGM13	WGM12	CS1		
$80	TCCR1A	COM1A		COM1B		-	-	WGM11	WGM10
$7F	DIDR1	-	-	-	-	-	-	AIN1D	AIN0D
$7E	DIDR0	ADC7D	ADC6D	ADC5D	ADC4D	ADC3D	ADC2D	ADC1D	ADC0D
$7D	ADTMR	GAIN		-	-	-	ADTM		
$7C	ADMUX	REFS		ADLAR	-	MUX			
$7B	ADCSRB	-	ACME	-	ICTL	-	ADTS		
$7A	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS		
$79	ADCH	ADC Data High							
$78	ADCL	ADC Data Low							
$77	EEDRH	EEPROM Data High							
$75	IVBASE	Interrupt Vector Base Address							
$70	TIMSK2	-	-	-	-	-	OCIE2B	OCIE2A	TOIE2
$6F	TIMSK1	-	-	ICIE1	-	-	OCIE1B	OCIE1A	TOIE1
$6E	TIMSK0	-	-	-	-	-	OCIE0B	OCIE0A	TOIE0
$6D	PCMSK2	PCINT[23:16]							
$6C	PCMSK1	PCINT[15:8]							
$6B	PCMSK0	PCINT[7:0]							
$69	EICRA	-	-	-	-	ISC1		ISC0	
$68	PCICR	-	-	-	-	-	PCIE2	PCIE1	PCIE0
$66	OSCCAL	-	-	OSC Calibration					
$65	PRR1	-	-	PRWDT	-	-	PREFL	PRPCI	-
$64	PRR	PRTWI	PRTIM2	PRTIM0	-	PRTIM1	PRSPI	PRUSART0	PRADC

$62	VDTCR	VDTCE	SWRSTN	-	-	-	VDTSEL		VDTEN
$61	CLKPR	CLKPCE	CLKOEN 0	CLKOEN 1	-	CLKPS			
$60	WDTCSR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0
$5F($3F)	SREG	I	T	H	S	V	N	Z	C
$5E($3E)	SPH	Stack point high byte							
$5D($3D)	SPL	Stack point low byte							
$55($35)	MCUCR	-	BODS	BODSE	PUD	-	-	IVSEL	IVCE
$54($34)	MCUSR	SWDD	-	-	OCDRF	WDRF	BORF	EXTRF	PORF
$53($33)	SMCR	-	-	-	-	SM			SE
$50($30)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS	
$4E(0x2E)	SPDR	SPI Data Register							
$4D($2D)	SPSR	SPIF	WCOL	-	-	-	DUAL	-	SPI2X
$4C($2C)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR	
$4B($2B)	GPIOR2	General purpose I/O register 2							
$4A($2A)	GPIOR1	General purpose I/O register 1							
$48($28)	OCR0B	Timer/counter 0 output compare register B							
$47($27)	OCR0A	Timer/counter 0 output compare register A							
$46($26)	TCNT0	Timer/Counter 0 counter							
$45($25)	TCCR0B	FOC0A	FOC0B	OC0AS	-	WGM02	CS0		
$44($24)	TCCR0A	COM0A		COM0B		-	-	WGM01	WGM00
$43($23)	GTCCR	TSM	-	-	-	-	-	PSRASY	PSRSYNC
$42($22)	EEARH	EEPROM Address high byte							
$41($21)	EEARL	EEPROM Address low byte							
$40($20)	EEDR	EEPROM Data							
$3F($1F)	EECR	EEPM2	-	EEPM1	EEPM0	EERIE	EEMWE	EEWE	EERE
$3E($1E)	GPIOR0	General purpose IO register 0							
$3D($1D)	EIMSK	-	-	-	-	-	-	INT1	INT0
$3C($1C)	EIFR	-	-	-	-	-	-	INTF1	INTF0
$3B($1B)	PCIFR	-	-	-	-	-	PCIF2	PCIF1	PCIF0
$37($17)	TIFR2	-	-	-	-	-	OCF2B	OCF2A	TOV2
$36($16)	TIFR1	-	-	ICF1	-	-	OCF1B	OCF1A	TOV1
$35($15)	TIFR0	-	-	-	-	-	OCF0B	OCF0A	TOV0
$2B($0B)	PORTD	Port output D							
$2A($0A)	DDRD	Data direction D							
$29($09)	PIND	Port input D							
$28($08)	PORTC	Port output C							

$27($07)	DDRC	Port direction C
$26($06)	PINC	Port input C
$25($05)	PORTB	Port output B
$24($04)	DDRB	Port direction B
$23($03)	PINB	Port input B

INSTRUCTION INDEX

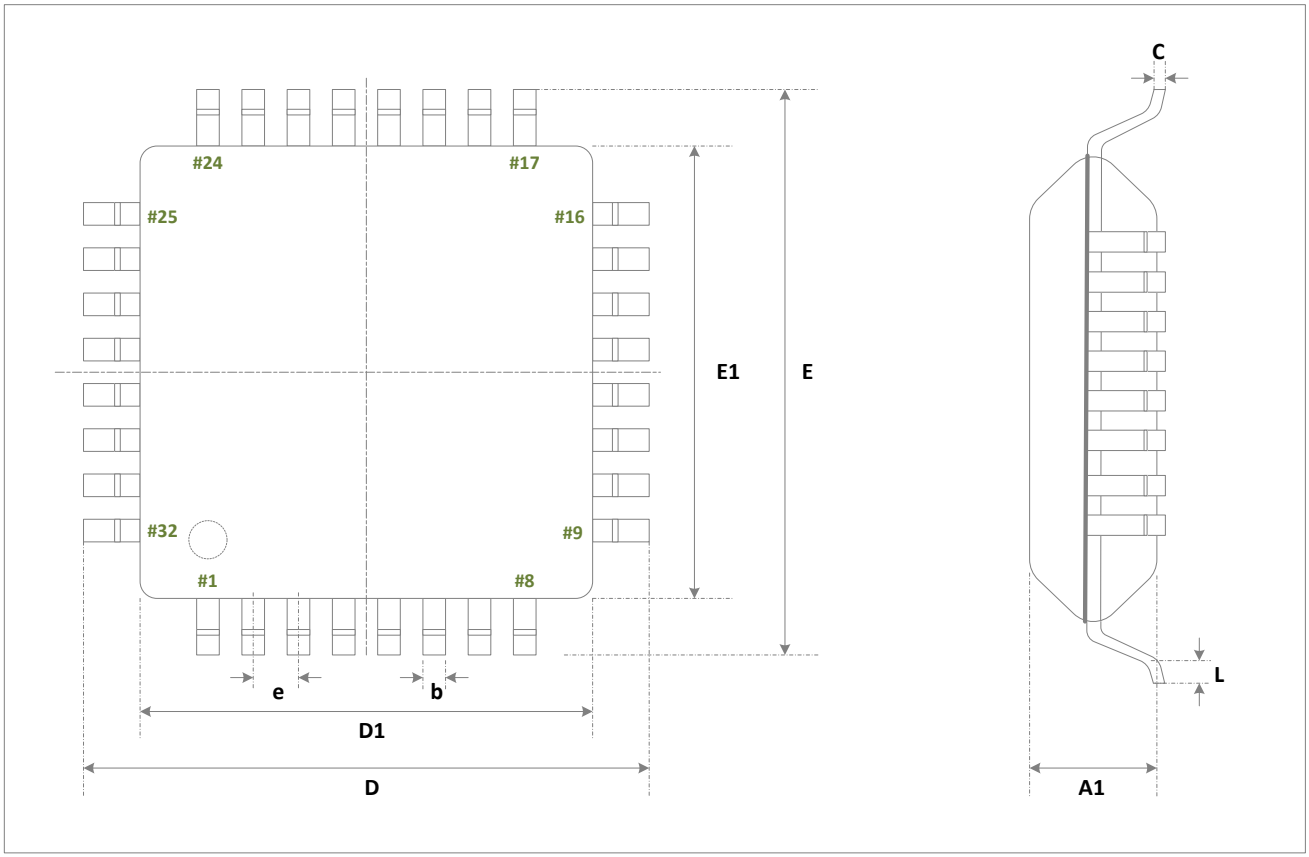
INST.	OPC.	FUNCITONS	OPERATION	FLAG	CYCLE
Arithmetic and Logic operation					
ADD	R_d, R_r	Add two registers	$R_d \leftarrow R_d + R_r$	Z,C,N,V,H	1
ADC	R_d, R_r	Add with carry two regiters	$R_d \leftarrow R_d + R_r + C$	Z,C,N,V,H	1
ADIW	R_{dl}, K	Add immediate to word	$R_{dh}:R_{dl} \leftarrow R_{dh}:R_{dl} + K$	Z,C,N,V,S	1
SUB	R_d, R_r	Subtract two registers	$R_d \leftarrow R_d - R_r$	Z,C,N,V,H	1
SUBI	R_d, K	Subtract constant from registers	$R_d \leftarrow R_d - K$	Z,C,N,V,H	1
SBC	R_d, R_r	Subtract with carry	$R_d \leftarrow R_d - R_r - C$	Z,C,N,V,H	1
SBCI	R_d, K	Subtract with carry constant	$R_d \leftarrow R_d – K - C$	Z,C,N,V,H	1
SBIW	R_{dl}, K	Subtract immediate from word	$R_{dh}:R_{dl} \leftarrow R_{dh}:R_{dl} - K$	Z,C,N,V,S	1
AND	R_d, R_r	Logical AND	$R_d \leftarrow R_d \& R_r$	Z,N,V	1
ANDI	R_d, K	Logical AND register and constant	$R_d \leftarrow R_d \& K$	Z,N,V	1
OR	R_d, R_r	Logical OR	$R_d \leftarrow R_d \mid R_r$	Z,N,V	1
ORI	R_d, K	Logical OR register and constant	$R_d \leftarrow R_d \mid K$	Z,N,V	1
EOR	R_d, R_r	Exclusive OR	$R_d \leftarrow R_d \oplus R_r$	Z,N,V	1
COM	R_d	One’s complement	$R_d \leftarrow \$FF - R_d$	Z,C,N,V	1
NEG	R_d	Two’s complement	$R_d \leftarrow \$00 - R_d$	Z,C,N,V,H	1
SBR	R_d, K	Set bit(s) in Register	$R_d \leftarrow R_d$ v K	Z,N,V	1
CBR	R_d, K	Clear bit(s) in Rigister	$R_d \leftarrow R_d$ v ($FF – K)	Z,N,V	1
INC	R_d	Increment	$R_d \leftarrow R_d + 1$	Z,N,V	1
DEC	R_d	Decrement	$R_d \leftarrow R_d - 1$	Z,N,V	1
TST	R_d	Test for zero or minus	$R_d \leftarrow R_d \& R_d$	Z,N,V	1
CLR	R_d	Clear register	$R_d \leftarrow R_d \oplus R_d$	Z,N,V	1
SER	R_d	Set register	$R_d \leftarrow \$FF$	None	1
MUL	R_d, R_r	Multiply unsigned	R_1: $R_0 \leftarrow R_d \times R_r$	Z,C	1
MULS	R_d, R_r	Multiply signed	R_1: $R_0 \leftarrow R_d \times R_r$	Z,C	1
MULSU	R_d, R_r	Multiply signed with unsigned	R_1: $R_0 \leftarrow R_d \times R_r$	Z,C	1
FMUL	R_d, R_r	Fractional MUL	R_1: $R_0 \leftarrow (R_d \times R_r) << 1$	Z,C	1
FMULS	R_d, R_r	Fractional MULS	R_1: $R_0 \leftarrow (R_d \times R_r) << 1$	Z,C	1
FMULSU	R_d, R_r	Fractional MULSU	R_1: $R_0 \leftarrow (R_d \times R_r) << 1$	Z,C	1
Branch Instructions					
RJMP	K	Relative jump	PC ← PC + K + 1	None	1
IJMP		Indirect jump to (Z)	PC ← Z	None	2
JMP	K	Direct jump	PC ← K	None	2
RCALL	K	Relative subroutine call	PC ← PC + K + 1	None	1
ICALL		Indirect call to (Z)	PC ← Z	None	2
CALL	K	Direct subroutine call	PC ← K	None	2
RET		Subroutine return	PC ← Stack	None	2
RETI		Interrupt return	PC ← Stack	I	2

INST.	OPC.	FUNCITONS	OPERATION	FLAG	CYCLE
Branch Instructions (Cont'd)					
CPSE	R_d, R_r	Compare, skip if equal	If(R_d=R_r) PC ← PC + 2 or 3	None	1/2
CP	R_d, R_r	Compare	R_d - R_r	Z,N,V,C,H	1
CPC	R_d, R_r	Compare with carry	R_d - R_r – C	Z,N,V,C,H	1
CPI	R_d, K	Compare with immediate	R_d - K	Z,N,V,C,H	1
SBRC	R_r, b	Skip if bit in register cleared	If(R_r(b)=0) PC ← PC + 2 or 3	None	1/2
SBRS	R_r, b	Skip if bit in register set	If(R_r(b)=1) PC ← PC + 2 or 3	None	1/2
SBIC	P, b	Skip if bit in I/O cleared	If(P(b)=0) PC ← PC + 2 or 3	None	1/2
SBIS	P, b	Skip if bit in I/O set	If(P(b)=1) PC ← PC + 2 or 3	None	1/2
BRBS	s, k	Branch if status flag set	If(SREG(S)=1) PC ← PC + K + 1	None	1/2
BRBC	s, k	Branch if status flag cleared	If(SREG(S)=0) PC ← PC + K + 1	None	1/2
BREQ	k	Branch if equal	if (Z = 1) then PC ← PC + k + 1	None	1/2
BRNE	k	Branch if not equal	if (Z = 0) then PC ← PC + k + 1	None	1/2
BRCS	k	Branch if carry set	if (C = 1) then PC ← PC + k + 1	None	1/2
BRCC	k	Branch if carry cleared	if (C = 0) then PC ← PC + k + 1	None	1/2
BRSH	k	Branch if same or higher	if (C = 0) then PC ← PC + k + 1	None	1/2
BRLO	k	Branch if lower	if (C = 1) then PC ← PC + k + 1	None	1/2
BRMI	k	Branch if minus	if (N = 1) then PC ← PC + k + 1	None	1/2
BRPL	k	Branch if plus	if (N = 0) then PC ← PC + k + 1	None	1/2
BRGE	k	Branch if greater or equal, signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1/2
BRLT	k	Branch if less than zerio, signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1/2
BRHS	k	Branch if half carry flag set	if (H = 1) then PC ← PC + k + 1	None	1/2
BRHC	k	Branch if half carry flag cleared	if (H = 0) then PC ← PC + k + 1	None	1/2
BRTS	k	Branch if T flag set	if (T = 1) then PC ← PC + k + 1	None	1/2
BRTC	k	Branch if T flag cleared	if (T = 0) then PC ← PC + k + 1	None	1/2
BRVS	k	Branch if overflow flag is set	f (V = 1) then PC ← PC + k + 1	None	1/2
BRVC	k	Branch if overflow flag cleared	f (V = 0) then PC ← PC + k + 1	None	1/2
BRIE	k	Branch if interrupt enabled	f (I = 1) then PC ← PC + k + 1	None	1/2
BRID	k	Branch if interrupt disabled	f (I = 0) then PC ← PC + k + 1	None	1/2
DATA TRANSFER Instructions					
MOV	Rd, Rr	Move between registers	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy register word	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load immediate	Rd ← K	None	1
LD	Rd, X	Load indirect	Rd ← (X)	None	1
LD	Rd, X+	Load indirect and post-inc.	Rd ← (X), X ← X + 1	None	1
LD	Rd, -X	Load indirect and pre-dec	X ← X - 1, Rd ← (X)	None	1
LD	Rd, Y	Load indirect	Rd ← (Y)	None	1
LD	Rd, Y+	Load indirect and post-inc	Rd ← (Y), Y ← Y + 1	None	1
LD	Rd, -Y	Load indirect and pre-dec	Y ← Y - 1, Rd ← (Y)	None	1
LDD	Rd, Y+q	Load indirect with displacement	Rd ← (Y + q)	None	1

LD	Rd, Z	Load indirect	Rd ← (Z)	None	1
LD	Rd, Z+	Load indirect and post-inc	Rd ← (Z), Z ← Z+1	None	1
LD	Rd, -Z	Load indirect and pre-dec	Z ← Z - 1, Rd ← (Z)	None	1
LDD	Rd, Z+q	Load indirect with displacement	Rd ← (Z + q)	None	1
LDS	Rd, k	Load direct from SRAM	Rd ← (k)	None	2
ST	X, Rr	Store indirect	(X) ← Rr	None	1
ST	X+, Rr	Store indirect and post-inc	(X) ← Rr, X ← X + 1	None	1
ST	-X, Rr	Store indirect and pre-dec	X ← X - 1, (X) ← Rr	None	1
ST	Y, Rr	Store indirect	(Y) ← Rr	None	1
ST	Y+, Rr	Store indirect and post-inc	(Y) ← Rr, Y ← Y + 1	None	1
ST	-Y, Rr	Store indirect and pre-dec	Y ← Y - 1, (Y) ← Rr	None	1
STD	Y+q, Rr	Store indirect with displacement	(Y + q) ← Rr	None	1
ST	Z, Rr	Store indirect	(Z) ← Rr	None	1
ST	Z+, Rr	Store indirect and post-inc	(Z) ← Rr, Z ← Z + 1	None	1
ST	-Z, Rr	Store indirect and pre-dec	Z ← Z - 1, (Z) ← Rr	None	1
STD	Z+q, Rr	Store indirect with displacement	(Z + q) ← Rr	None	1
STS	k, Rr	Store direct	(k) ← Rr	None	2
LPM		Load program memory	R0 ← (Z)	None	2
LPM	Rd, Z	Load program memory	Rd ← (Z)	None	2
LPM	Rd, Z+	Load program and post-inc	Rd ← (Z), Z ← Z+1	None	2
LD	Rd, Z+	Load	Rd ← (Z), Z ← Z+1	None	1
LD	Rd, -Z	Load indirect and pre-dec	Z ← Z - 1, Rd ← (Z)	None	1
LDD	Rd, Z+q	Load indirect with displacement	Rd ← (Z + q)	None	1
LDS	Rd, k	Load direct from SRAM	Rd ← (k)	None	2
IN	Rd, P	In port	Rd ← P	None	1
OUT	P, Rr	Out port	P ← Rr	None	1
PUSH	Rr	Push register on stack	STACK ← Rr	None	1
POP	Rd	Pop register from stack	Rd ← STACK	None	1
BIT and BIT-TEST Instructions					
SBI	P, b	Set bit in I/O register	I/O(P, b) ← 1	None	1
CBI	P, b	Clear bit in I/O register	I/O(P, b) ← 0	None	1
LSL	Rd	Logical shift left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z,C,N,V	1
LSR	Rd	Logical shift right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z	1
ROL	Rd	Rotate left through carry	Rd(0)←C, Rd(n+1) ← Rd(n), C←Rd(7)	Z	1
ROR	Rd	Rotate right through carry	Rd(7)←C, Rd(n) ← Rd(n+1), C←Rd(0)	Z	1
ASR	Rd	Arithmetic shift right	Rd(n) ← Rd(n+1), n=0:6	Z	1
SWAP	Rd	Swap nibbles	Rd(3:0) ← Rd(7:4), Rd(7:4) ← Rd(3:0)	None	1
BSET	s	Flag set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag clear	SREG(s) ← 0	SREG(s)	1
BST	Rr, b	Bit store from register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1

CLC		Clear carry	C ← 0	C	1
SEN		Set negative flag	N ← 1	N	1
CLN		Clar negative flag	N ← 0	N	1
SEZ		Set zero flag	Z ← 1	Z	1
CLZ		Clear zero flag	Z ← 0	Z	1
SEI		Global interrupt enable	I ← 1	I	1
CLI		Global interrupt disable	I ← 0	I	1
SES		Set signed test flag	S ← 1	S	1
CLS		Clear signed test flag	S ← 0	S	1
SEV		Set 2’s complement overflow	V ← 1	V	1
CLV		Clear 2’s complement overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
MCU Control Instructions					
NOP		No operation		None	1
SLEEP		Sleep		None	1
WDR		Watchdog reset		None	1
BREAK		Software break	Only for debug purpose	None	N/A

Package Definitions



LQFP32L Dimension

Simboly	Min.	Typical.	Max.	Unit
D	8.90	9.00	9.10	mm
D1	6.90	7.00	7.10	mm
b	0.15	0.20	0.25	mm
e	0.75	0.80	0.85	mm
E	8.90	9.00	9.10	mm
E1	6.90	7.00	7.10	mm
C	-	0.10	-	mm
L	0.55	0.60	0.65	mm
A1	-	1.40	-	mm